Multifunction-I/O-X3 series
Register-Map
Reference

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1.Overview

This document summarizes the register map and communication method for Multifunction I / O-X3 series and Infrasound sensor. It corresponds to **ADXIII42LE-Ethernet, ADXIII42LE-CORE, ADXIII-INF01LE, and ADXIII-INF04LE.**

2. Physical means of data communication

The physical means of data communication with **ADXIII42LE-Ethernet**, **ADXIII42LE-CORE** and **ADXIII-INF01LE** correspond to the following 4 methods. All of them are shipped with exclusive implementation according to the hardware order, so it is not possible to switch with one hardware. The register map and communication frame structure are the same regardless of which method is used.

ETHERNET	TCP/IP (This product is server operation)
ETHERNET	UDP (This product is server operation)
UART	RS232C,921.6Kbps,Data8bit NonParity,Stop2bit
UART	LVTTL,921.6Kbps,Data8bit NonParity,Stop2bit

The physical means of data communication with **ADXIII-INF04LE** is The following 3 methods are switched using a jumper. Specify only TCP / UDP when ordering. The register map and communication frame structure are the same regardless of which method is used.

ETHERNET	TCP/IP or UDP (This product is server operation)
UART	RS232C,921.6Kbps,Data8bit NonParity,Stop2bit
UART	RS232C,115.2Kbps,Data8bit NonParity,Stop2bit

3. Frame structure

There are four frame structures. There is only one type of writing. There are three types of reading, block read and ring buffer read, in addition to normal single read. The frame structure is shown below. Green is a variable, red is a fixed, blue is a meaningless bit field.

Write

host → target(6Byte)

D31 to 0 are write data, and A4 to A0 are register numbers. The leading BIT4 to 7 means a write command. X is an invalid bit and has no meaning.

	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
BYTE0	D7	D15	D23	D31(MSB)	0	0	1	1
BYTE1	D0(LSB)	D1	D2	D3	D4	D5	D6	X
BYTE2	D8	D9	D10	D11	D12	D13	D14	X
BYTE3	D16	D17	D18	D19	D20	D21	D22	X
BYTE4	D24	D25	D26	D27	D28	D29	D30	X
BYTE5	A0(LSB)	A1	A2	A3	A4(MSB)	X	X	X

Read (single)

host → target(1Byte)

A4 to A0 are register numbers. Leading BIT5 to 7 means read command.

	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
BYTE0	A0(LSB)	A1	A2	A3	A4(MSB)	1	1	1

Target → Host (4Byte)

D31 to D0 are reading data.

	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
BYTE0	D0(LSB)	D1	D2	D3	D4	D5	D6	D7
BYTE1	D8	D9	D10	D11	D12	D13	D14	D15
BYTE2	D16	D17	D18	D19	D20	D21	D22	D23
BYTE3	D24	D25	D26	D27	D28	D29	D30	D31(MSB)

Read (ring buffer)

Host → target(1Byte)

A4 to A0 are register numbers. Forehand BIT 5 to 7 means a read command. If 0 is specified for the register number here, reading from the ring buffer is performed. If a ring buffer interrupt has occurred, use this command to read ring buffer data.。

	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
BYTE0	A0(LSB)	A1	A2	A3	A4(MSB)	1	1	1

Target → Host(4108Byte)

One frame consists of 4108 bytes. It starts with a channel block consisting of 32 bytes. This channel block is

1. 16-bit analog input data channel 0 (hereinafter abbreviated as AI0) at the first 0-1 byte,
2. The lower 2 bytes of the 32-bit counter input data channel 0 (hereinafter abbreviated as CTC0) in the next 2-3 bytes
3. Analog input data channel 1 (hereinafter abbreviated as AI1) at the next 4-5 bytes
4. The upper two bytes of 32-bit counter input data channel 0 (hereafter abbreviated as CTC0) are stored in the next 6-7 bytes, and this is continued for all channels.
5. The next 8-9 bytes are AI2,
6. 11-11 bytes The lower 2 bytes of CTC1,
7. 12-13 bytes AI3,
8. 14-15 bytes upper 2 bytes of CTC1,
9. 16-17 bytes AI4,
10. 18-19 bytes The lower 2 bytes of CTC2,
11. 20-21 bytes AI5,
12. 22-23 bytes The upper two bytes of CTC2,
13. 24-25 bytes AI6,
14. 26-27 bytes Lower 2 bytes of CTC3,
15. 28-29 bytes 2 bytes of AI7,
16. The last 30-31 bytes cover all channels (A / D 8 channels, counter 4 channels) with the upper 2 bytes of CTC3.

Note that one 4-byte counter data is at intervals for 2 bytes each. In infrastructure sound mode, (in the case of ADXIII-INF01LE) Infrasound DC in CTC0, Infrasound AC in CTC1, temperature in CTC2, CTC3 becomes meaningless, (In the case of ADXIII-INF04LE) Infrasound LF in CTC0, temperature in CTC1, CTC2 and CTC3 are meaningless. This 32-byte channel block is repeated 128 times continuously, transferring 128 samples of 8 channels of 16-bit A / D data and 4 channels of 32-bit counter data. Finally, 12 bytes of temperature, GPS data and DI data are added. In the following data, Bit 0 is LSB.

	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
BYTE0	AI0-Bit0(LSB)	AI0-Bit1	AI0-Bit2	AI0-Bit3	AI0-Bit4	AI0-Bit5	AI0-Bit6	AI0-Bit7
BYTE1	AI0-Bit8	AI0-Bit9	AI0-Bit10	AI0-Bit11	AI0-Bit12	AI0-Bit13	AI0-Bit14	AI0-Bit15(MSB)
BYTE2	CTC0-Bit0(LSB)	CTC0-Bit1	CTC0-Bit2	CTC0-Bit3	CTC0-Bit4	CTC0-Bit5	CTC0-Bit6	CTC0-Bit7
BYTE3	CTC0-Bit8	CTC0-Bit9	CTC0-Bit10	CTC0-Bit11	CTC0-Bit12	CTC0-Bit13	CTC0-Bit14	CTC0-Bit15
BYTE4	AI1-Bit0(LSB)	AI1-Bit1	AI1-Bit2	AI1-Bit3	AI1-Bit4	AI1-Bit5	AI1-Bit6	AI1-Bit7
BYTE5	AI1-Bit8	AI1-Bit9	AI1-Bit10	AI1-Bit11	AI1-Bit12	AI1-Bit13	AI1-Bit14	AI1-Bit15(MSB)

BYTE6	CTC0-Bit16	CTC0-Bit17	CTC0-Bit18	CTC0-Bit19	CTC0-Bit20	CTC0-Bit21	CTC0-Bit22	CTC0-Bit23
BYTE7	CTC0-Bit24	CTC0-Bit25	CTC0-Bit26	CTC0-Bit27	CTC0-Bit28	CTC0-Bit29	CTC0-Bit30	CTC0-Bit31(MSB)
BYTE8	AI2-Bit0(LSB)	AI2-Bit1	AI2-Bit2	AI2-Bit3	AI2-Bit4	AI2-Bit5	AI2-Bit6	AI2-Bit7
BYTE9	AI2-Bit8	AI2-Bit9	AI2-Bit10	AI2-Bit11	AI2-Bit12	AI2-Bit13	AI2-Bit14	AI2-Bit15(MSB)
BYTE10	CTC1-Bit0(LSB)	CTC1-Bit1	CTC1-Bit2	CTC1-Bit3	CTC1-Bit4	CTC1-Bit5	CTC1-Bit6	CTC1-Bit7
BYTE11	CTC1-Bit8	CTC1-Bit9	CTC1-Bit10	CTC1-Bit11	CTC1-Bit12	CTC1-Bit13	CTC1-Bit14	CTC1-Bit15
BYTE12	AI3-Bit0(LSB)	AI3-Bit1	AI3-Bit2	AI3-Bit3	AI3-Bit4	AI3-Bit5	AI3-Bit6	AI3-Bit7
BYTE13	AI3-Bit8	AI3-Bit9	AI3-Bit10	AI3-Bit11	AI3-Bit12	AI3-Bit13	AI3-Bit14	AI3-Bit15(MSB)
BYTE14	CTC1-Bit16	CTC1-Bit17	CTC1-Bit18	CTC1-Bit19	CTC1-Bit20	CTC1-Bit21	CTC1-Bit22	CTC1-Bit23
BYTE15	CTC1-Bit24	CTC1-Bit25	CTC1-Bit26	CTC1-Bit27	CTC1-Bit28	CTC1-Bit29	CTC1-Bit30	CTC1-Bit31(MSB)
BYTE16	AI4-Bit0(LSB)	AI4-Bit1	AI4-Bit2	AI4-Bit3	AI4-Bit4	AI4-Bit5	AI4-Bit6	AI4-Bit7
BYTE17	AI4-Bit8	AI4-Bit9	AI4-Bit10	AI4-Bit11	AI4-Bit12	AI4-Bit13	AI4-Bit14	AI4-Bit15(MSB)
BYTE18	CTC2-Bit0(LSB)	CTC2-Bit1	CTC2-Bit2	CTC2-Bit3	CTC2-Bit4	CTC2-Bit5	CTC2-Bit6	CTC2-Bit7
BYTE19	CTC2-Bit8	CTC2-Bit9	CTC2-Bit10	CTC2-Bit11	CTC2-Bit12	CTC2-Bit13	CTC2-Bit14	CTC2-Bit15
BYTE20	AI5-Bit0(LSB)	AI5-Bit1	AI5-Bit2	AI5-Bit3	AI5-Bit4	AI5-Bit5	AI5-Bit6	AI5-Bit7
BYTE21	AI5-Bit8	AI5-Bit9	AI5-Bit10	AI5-Bit11	AI5-Bit12	AI5-Bit13	AI5-Bit14	AI5-Bit15(MSB)
BYTE22	CTC2-Bit16	CTC2-Bit17	CTC2-Bit18	CTC2-Bit19	CTC2-Bit20	CTC2-Bit21	CTC2-Bit22	CTC2-Bit23
BYTE23	CTC2-Bit24	CTC2-Bit25	CTC2-Bit26	CTC2-Bit27	CTC2-Bit28	CTC2-Bit29	CTC2-Bit30	CTC2-Bit31(MSB)
BYTE24	AI6-Bit0(LSB)	AI6-Bit1	AI6-Bit2	AI6-Bit3	AI6-Bit4	AI6-Bit5	AI6-Bit6	AI6-Bit7
BYTE25	AI6-Bit8	AI6-Bit9	AI6-Bit10	AI6-Bit11	AI6-Bit12	AI6-Bit13	AI6-Bit14	AI6-Bit15(MSB)
BYTE26	CTC3-Bit0(LSB)	CTC3-Bit1	CTC3-Bit2	CTC3-Bit3	CTC3-Bit4	CTC3-Bit5	CTC3-Bit6	CTC3-Bit7
BYTE27	CTC3-Bit8	CTC3-Bit9	CTC3-Bit10	CTC3-Bit11	CTC3-Bit12	CTC3-Bit13	CTC3-Bit14	CTC3-Bit15
BYTE28	AI7-Bit0(LSB)	AI7-Bit1	AI7-Bit2	AI7-Bit3	AI7-Bit4	AI7-Bit5	AI7-Bit6	AI7-Bit7
BYTE29	AI7-Bit8	AI7-Bit9	AI7-Bit10	AI7-Bit11	AI7-Bit12	AI7-Bit13	AI7-Bit14	AI7-Bit15(MSB)
BYTE30	CTC3-Bit16	CTC3-Bit17	CTC3-Bit18	CTC3-Bit19	CTC3-Bit20	CTC3-Bit21	CTC3-Bit22	CTC3-Bit23
BYTE31	CTC3-Bit24	CTC3-Bit25	CTC3-Bit26	CTC3-Bit27	CTC3-Bit28	CTC3-Bit29	CTC3-Bit30	CTC3-Bit31(MSB)
	†This 32 byte channel block is sequentially repeated 128 samples.							
BYTE4095	CTC3-Bit24	CTC3-Bit25	CTC3-Bit26	CTC3-Bit27	CTC3-Bit28	CTC3-Bit29	CTC3-Bit30	CTC3-Bit31(MSB)

Finally, GPS, temperature data and DI data are added at 12 bytes below.

BYTE4096	D0	D1	D2	D3	D4	D5	D6	D7
BYTE4097	D8	D9	D10	D11	D12	D13	D14	D15
BYTE4098	D16	D17	D18	D19	D20	D21	D22	D23
BYTE4099	D24	D25	D26	D27	D28	D29	D30	D31
BYTE4100	D0	D1	D2	D3	D4	D5	D6	D7
BYTE4101	D8	D9	D10	D11	D12	D13	D14	D15
BYTE4102	D16	D17	D18	D19	D20	D21	D22	D23
BYTE4103	D24	D25	D26	D27	D28	D29	D30	D31
BYTE4104	D0	D1	D2	D3	D4	D5	D6	D7
BYTE4105	D8	D9	D10	D11	D12	D13	D14	D15

BYTE4106	D16	D17	D18	D19	D20	D21	D22	D23
BYTE4107	D24	D25	D26	D27	D28	D29	D30	D31

<Description of auxiliary data>

Bit fields from 4096 to 4107 bytes are mapped as follows depending on the operation mode and model.

Infrasound mode (ADXIII-INF01LE)

BYTE4096～4099 , D15-0 temperature data (equivalent to signed short), D31-16, digital input.

BYTE4100～4103 , D 7-0 GPS time, D 15-8 GPS time, D 23-16 GPS time second, D 31-24 GPS time day.

BYTE4104～4107 , D11-0 GPS time millisecond, D 27-16 GPS time year, D 31-28 GPS time month.

Infrasound mode (ADXIII-INF04LE)

BYTE4096～4099 , D31-0 filled with 0.

BYTE4100～4103 , D 7-0 GPS time, D 15-8 GPS time, D 23-16 GPS time second, D 31-24 GPS time day.

BYTE4104～4107 , D11-0 GPS time millisecond, D 27-16 GPS time year, D 31-28 GPS time month.

In Multifunction I/O mode

BYTE4096～4099 , D15 to 0 temperature data (equivalent to signed short), D31 to 16 digital input.

BYTE4100～4103 , D23-0 Always 0, D31-24 Remaining battery.

BYTE4104～4107 , D31 to 0 Always 0.

*The remaining battery charge is% conversion when multiplying the value

of 8Bit above as unsigned straight binary by 1.2890625.

* The temperature data is ° C when it is multiplied by 0.03125 as a signed complement binary.

* When GPS is not connected, GPS related bit fields are meaningless.

Read (block)

host → target(1Byte)

A4 to A0 are register numbers. Forehead's BIT 5 to 7 means a read command. If 0x1F is specified as the register number here, it will be a block read. Unlike ring buffer, read at any time of host.

	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
BYTE0	A0(LSB)	A1	A2	A3	A4(MSB)	1	1	1

Target → Host (44Byte)

First, there is a channel block consisting of 32 bytes in forehead. This channel block consists of (1) 16-bit analog input data channel 0 ((Hereinafter abbreviated as "AI0")) in the first 0-1 bytes from the beginning, (2) the second 2-3 bytes are "AI1", (3) the next 4-5 bytes Is "AI2", (4) the next 6-7 bytes are "AI3", (5) the next 8-9 bytes are "AI4", (6) the next 10-11 bytes are "AI5", (7) The next 12-13 bytes are "AI6", (8) the next 14-15 bytes are "AI7", (9) the next 16th to 19th bytes are the 32-bit counter input data channel 0(Hereinafter abbreviated as "CTC0") , (10) The next 20-23 bytes are "CTC1", (11) the next 24-27 bytes are "CTC2", (12) the next 28-31 bytes are "CTC3" ... , Data is arranged.

(A/D 8 channels, 4 counters).

In Infrasound mode (for ADXIII-INF01LE) Infrasound DC in CTC0, Infrasound AC in CTC1, temperature in CTC2, CTC3 is meaningless, (In the case of ADXIII-INF04LE) Infrasound LF in CTC0, temperature in CTC1, CTC2 and CTC3 are meaningless. Unlike ring buffer mode, by 1 time of this 32-byte channel block transfers one sample of each of eight channels of 16-bit A / D data and four channels of 32-bit counter data. In the following data, Bit 0 is LSB.

	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7
BYTE0	AI0-Bit0(LSB)	AI0-Bit1	AI0-Bit2	AI0-Bit3	AI0-Bit4	AI0-Bit5	AI0-Bit6	AI0-Bit7
BYTE1	AI0-Bit8	AI0-Bit9	AI0-Bit10	AI0-Bit11	AI0-Bit12	AI0-Bit13	AI0-Bit14	AI0-Bit15(MSB)
BYTE2	CTC0-Bit0(LSB)	CTC0-Bit1	CTC0-Bit2	CTC0-Bit3	CTC0-Bit4	CTC0-Bit5	CTC0-Bit6	CTC0-Bit7
BYTE3	CTC0-Bit8	CTC0-Bit9	CTC0-Bit10	CTC0-Bit11	CTC0-Bit12	CTC0-Bit13	CTC0-Bit14	CTC0-Bit15
BYTE4	AI1-Bit0(LSB)	AI1-Bit1	AI1-Bit2	AI1-Bit3	AI1-Bit4	AI1-Bit5	AI1-Bit6	AI1-Bit7
BYTE5	AI1-Bit8	AI1-Bit9	AI1-Bit10	AI1-Bit11	AI1-Bit12	AI1-Bit13	AI1-Bit14	AI1-Bit15(MSB)
BYTE6	CTC0-Bit16	CTC0-Bit17	CTC0-Bit18	CTC0-Bit19	CTC0-Bit20	CTC0-Bit21	CTC0-Bit22	CTC0-Bit23
BYTE7	CTC0-Bit24	CTC0-Bit25	CTC0-Bit26	CTC0-Bit27	CTC0-Bit28	CTC0-Bit29	CTC0-Bit30	CTC0-Bit31(MSB)
BYTE8	AI2-Bit0(LSB)	AI2-Bit1	AI2-Bit2	AI2-Bit3	AI2-Bit4	AI2-Bit5	AI2-Bit6	AI2-Bit7
BYTE9	AI2-Bit8	AI2-Bit9	AI2-Bit10	AI2-Bit11	AI2-Bit12	AI2-Bit13	AI2-Bit14	AI2-Bit15(MSB)
BYTE10	CTC1-Bit0(LSB)	CTC1-Bit1	CTC1-Bit2	CTC1-Bit3	CTC1-Bit4	CTC1-Bit5	CTC1-Bit6	CTC1-Bit7
BYTE11	CTC1-Bit8	CTC1-Bit9	CTC1-Bit10	CTC1-Bit11	CTC1-Bit12	CTC1-Bit13	CTC1-Bit14	CTC1-Bit15
BYTE12	AI3-Bit0(LSB)	AI3-Bit1	AI3-Bit2	AI3-Bit3	AI3-Bit4	AI3-Bit5	AI3-Bit6	AI3-Bit7
BYTE13	AI3-Bit8	AI3-Bit9	AI3-Bit10	AI3-Bit11	AI3-Bit12	AI3-Bit13	AI3-Bit14	AI3-Bit15(MSB)
BYTE14	CTC1-Bit16	CTC1-Bit17	CTC1-Bit18	CTC1-Bit19	CTC1-Bit20	CTC1-Bit21	CTC1-Bit22	CTC1-Bit23
BYTE15	CTC1-Bit24	CTC1-Bit25	CTC1-Bit26	CTC1-Bit27	CTC1-Bit28	CTC1-Bit29	CTC1-Bit30	CTC1-Bit31(MSB)
BYTE16	AI4-Bit0(LSB)	AI4-Bit1	AI4-Bit2	AI4-Bit3	AI4-Bit4	AI4-Bit5	AI4-Bit6	AI4-Bit7
BYTE17	AI4-Bit8	AI4-Bit9	AI4-Bit10	AI4-Bit11	AI4-Bit12	AI4-Bit13	AI4-Bit14	AI4-Bit15(MSB)
BYTE18	CTC2-Bit0(LSB)	CTC2-Bit1	CTC2-Bit2	CTC2-Bit3	CTC2-Bit4	CTC2-Bit5	CTC2-Bit6	CTC2-Bit7
BYTE19	CTC2-Bit8	CTC2-Bit9	CTC2-Bit10	CTC2-Bit11	CTC2-Bit12	CTC2-Bit13	CTC2-Bit14	CTC2-Bit15
BYTE20	AI5-Bit0(LSB)	AI5-Bit1	AI5-Bit2	AI5-Bit3	AI5-Bit4	AI5-Bit5	AI5-Bit6	AI5-Bit7
BYTE21	AI5-Bit8	AI5-Bit9	AI5-Bit10	AI5-Bit11	AI5-Bit12	AI5-Bit13	AI5-Bit14	AI5-Bit15(MSB)
BYTE22	CTC2-Bit16	CTC2-Bit17	CTC2-Bit18	CTC2-Bit19	CTC2-Bit20	CTC2-Bit21	CTC2-Bit22	CTC2-Bit23
BYTE23	CTC2-Bit24	CTC2-Bit25	CTC2-Bit26	CTC2-Bit27	CTC2-Bit28	CTC2-Bit29	CTC2-Bit30	CTC2-Bit31(MSB)
BYTE24	AI6-Bit0(LSB)	AI6-Bit1	AI6-Bit2	AI6-Bit3	AI6-Bit4	AI6-Bit5	AI6-Bit6	AI6-Bit7
BYTE25	AI6-Bit8	AI6-Bit9	AI6-Bit10	AI6-Bit11	AI6-Bit12	AI6-Bit13	AI6-Bit14	AI6-Bit15(MSB)
BYTE26	CTC3-Bit0(LSB)	CTC3-Bit1	CTC3-Bit2	CTC3-Bit3	CTC3-Bit4	CTC3-Bit5	CTC3-Bit6	CTC3-Bit7
BYTE27	CTC3-Bit8	CTC3-Bit9	CTC3-Bit10	CTC3-Bit11	CTC3-Bit12	CTC3-Bit13	CTC3-Bit14	CTC3-Bit15
BYTE28	AI7-Bit0(LSB)	AI7-Bit1	AI7-Bit2	AI7-Bit3	AI7-Bit4	AI7-Bit5	AI7-Bit6	AI7-Bit7
BYTE29	AI7-Bit8	AI7-Bit9	AI7-Bit10	AI7-Bit11	AI7-Bit12	AI7-Bit13	AI7-Bit14	AI7-Bit15(MSB)
BYTE30	CTC3-Bit16	CTC3-Bit17	CTC3-Bit18	CTC3-Bit19	CTC3-Bit20	CTC3-Bit21	CTC3-Bit22	CTC3-Bit23
BYTE31	CTC3-Bit24	CTC3-Bit25	CTC3-Bit26	CTC3-Bit27	CTC3-Bit28	CTC3-Bit29	CTC3-Bit30	CTC3-Bit31(MSB)

Finally, 12 bytes of temperature, GPS data and DI data are added.

BYTE32	D0	D1	D2	D3	D4	D5	D6	D7
BYTE33	D8	D9	D10	D11	D12	D13	D14	D15
BYTE34	D16	D17	D18	D19	D20	D21	D22	D23
BYTE35	D24	D25	D26	D27	D28	D29	D30	D31
BYTE36	D0	D1	D2	D3	D4	D5	D6	D7

BYTE37	D8	D9	D10	D11	D12	D13	D14	D15
BYTE38	D16	D17	D18	D19	D20	D21	D22	D23
BYTE39	D24	D25	D26	D27	D28	D29	D30	D31
BYTE40	D0	D1	D2	D3	D4	D5	D6	D7
BYTE41	D8	D9	D10	D11	D12	D13	D14	D15
BYTE42	D16	D17	D18	D19	D20	D21	D22	D23
BYTE43	D24	D25	D26	D27	D28	D29	D30	D31

<Description of auxiliary data>

Bitfields of 32 to 43 bytes are mapped as follows depending on the operation mode and model.

Infrasound mode (ADXIII-INF01LE)

BYTE 32-35 , D15-0 temperature data (equivalent to signed short), D31-16 Digital input

BYTE 36-39 , D7-0 GPS time, D15-8 GPS time minutes, D23-16 GPS time seconds, D31-24 GPS time day

BYTE 40-43 , D11-0 GPS time millisecond, D27-16 GPS time year, D31-28 GPS time month

Infrasound mode (ADXIII-INF04LE)

BYTE 32-35 , Filled with D31-0 0

BYTE 36-39 , D7-0 GPS time, D15-8 GPS time minutes, D23-16 GPS time seconds, D31-24 GPS time day

BYTE 40-43 , D11-0 GPS time millisecond, D27-16 GPS time year, D31-28 GPS time month

In Multifunction I / O mode

BYTE 32-35 , D15-0 temperature data (equivalent to signed short),D31-16 Digital input

BYTE 36-39 , D23-0 Always 0, D31-24 battery remaining amount

BYTE 40-43 , D31-0 Always 0

* The remaining battery charge is% conversion when multiplying the value of 8Bit above as unsigned straight binary by 1.2890625.

* The temperature data is ° C when it is multiplied by 0.03125 as a signed complement binary.

* When GPS is not connected, GPS related bit fields are meaningless.

4. Signal conditioning

The acquired analog data and infrastructure sound data are scaled as follows. Please note that in the Infrasound model, input channel assignments are fixed.

ADXⅢ-INF01LE	Before conversion	After conversion	Unit	
Acceleration XYZ (AI0-2)	0-65535	0-3347	gal	
Sound Noise Level(Z) (AI3)	0-39999	10-110	dB	
barometer (AI4)	2789-65535	15-115	KPa	
1PPS (AI5)	0-65535	0-4095	mV	(same as 4.096 V)
Infrasound DC（CTC0）	14680064-18874368	±733413.5 mPa		
Infrasound AC（CTC1）	14680064-18874368	±733413.5 mPa		
Temperature（CTC2）	0-2097151	0-81.92	℃	

ADXⅢ-INF04LE	Before conversion	After conversion	Unit	
Acceleration XYZ (AI0-2)	0-65535	0-3347	gal	
Infrasound HF (AI3)	0-65535	±71050	mPa	
Power supply voltage(AI4)	0-65535	0-16384	mV	
1PPS (AI5)	0-65535	0-4095	mV	(same as 4.096 V)
Infrasound LF(CTC0)	0-4294967294	0-1048575.9995	hPa	
Temperature(CTC1)	0-4294967294	0-42949672.94	℃	

Common	Before conversion	After conversion	Unit
Voltage ±10V	0-65535	±10	V
Voltage ±1V	0-65535	±1	V
Voltage ±100mV	0-65535	±100	mV
Voltage ±10mV	0-65535	±10	mV
Voltage 4.096V	0-65535	0-4095	mV

The amp is the top five scales. Besides, it can operate Pt, JPt and strain gauges with a 2mA current source. In the case of 4-20 mA, the voltage value by resistance, and in the case of thermocouple, the electromotive force is converted by the scale of the above-mentioned amplifier. In the case of a thermocouple, perform linearization with software. For zero junction compensation, temperature data is added in block read and ring buffer read. So please use this.

5.Definition of register number

There are the following 18 registers.
Specify the following register numbers for 5 bits of A4 to A0 in each frame structure.

```
#define   RING_BUFFER_IO   0x0
#define   SETCLOCK 0x1
#define   TRIG1            0x2
#define   TRIG2            0x3
#define   TRIG3            0x4
#define   TRIG4            0x5
#define   SETAO            0x6
#define   COUNTER          0x7
#define   DO               0x8
#define   DI_MASK          0x9
#define   DI_PATT          0xA
#define   DEADTIME_PH      0xB
#define   BANK_CTC_ADDR    0xC
#define   SCP1             0xD
#define   SCP3             0xE
#define   STATUS           0XF
#define   LAST_BANK        0x10
#define   INFRS_PACK       0x1F
```

6.Register contents

[RW] is a read / write register and [RO] is a read only register.

SETCLOCK [RW] **Required**

Bit24～0 Set the sampling frequency. Sampling frequency = 480.8 KHz / SET CLOCK. The valid range is 0x17 to 0x1FFFFFF. Determines the sampling of the ring buffer. In the case of polling, make this sampling sufficiently faster than the polling period.

Default 0x7FFF

TRIG1 [RW]

Bit31～16 Stop trigger trigger delay.
Data acquisition is stopped with a delay of 1/8 sample x set value.

Bit15～0 Trigger delay for start trigger.
Data acquisition is started with a delay of 1/8 sample x set value.

Default 0x0

TRIG2 [RW]

Bit31～16	Trigger level 2 for analog start trigger. The analog level minimum to maximum correspond to 0 to 0xFFFF.
Bit15～0	Trigger level 1 for analog start trigger. The analog level minimum to maximum correspond to 0 to 0xFFFF.
Default	0x0

TRIG3 [RW]

Bit31～16	Trigger level 2 for analog stop trigger. The analog level minimum to maximum correspond to 0 to 0xFFFF.
Bit15～0	Trigger level 1 for analog stop trigger. The analog level minimum to maximum correspond to 0 to 0xFFFF.
Default	0

TRIG4 [RW] **Required**

Bit31	Stop counter valid at 1 and 0 invalid
Bit30～19	Stop size of the stop counter. One bank is shown per one value.
Bit18	Enable digital filter (4th order moving average) for analog input at 1. Invalid with 0.
Bit17	Infra sound mode in 1, normal data acquisition mode in 0.
Bit16～13	Channel designation for digital input edge / stand top trigger. Specify one of DI 0-15 with 0-15.
Bit12～9	Designation of digital input edge / start trigger channel. Specify one of DI 0-15 with 0 to 15.
Bit8	Triggering buffer is enabled (RUN) at 1 and invalid (STOP) at 0.
Bit7～4	Specify a stop trigger. Please select from the following seven. 0x0 : Trigger is not established. 0x1 : Unconditional trigger. 0x2 : Trigger on rising edge of digital input. 0x3 : Trigger on falling edge of digital input. 0x4 : Trigger when digital input has specified pattern. 0xB : Level (edge) trigger of analog input. 0xC : Area trigger of analog input.
Bit3～0	Specify a start trigger. Please select from the following seven. 0x0 : Trigger is not established. 0x1 : Unconditional trigger. 0x2 : Trigger on rising edge of digital input. 0x3 : Trigger on falling edge of digital input. 0x4 : Trigger when digital input has specified pattern. 0xB : Level (edge) trigger of analog input. 0xC : Area trigger of analog input.
Default	0x0

DI_MASK [RW]

Bit31～16	Set the mask for DI pattern trigger (stop trigger).
Bit15～0	Set the mask for DI pattern trigger (start trigger).
Default	0x0

DI_PATT [RW]

Bit31～16	Set the pattern in DI pattern trigger (stop trigger).
Bit15～0	Set the pattern in DI pattern trigger (start trigger).
Default	0x0

DEADTIME_PH [RW]

Bit31～24	Set to 1 to enable the peak hold function. When the data is read, the hold is cleared. It is a function to not miss the instantaneous value. The bit field represents the channel. ***[Required for acceleration and noise when polling with infrasound = set only AI0-3 to 1]***
Bit23～0	Specify the time until the stop trigger detection becomes effective after the start trigger is effective. Sudden stop trigger is detected after start trigger detection It is a function to prevent it from getting stuck. The value is 1/8 sample number.
Default	0x0

BANK_CTC_ADDR [RO]

Bit31	Ring buffer interrupt occurred (read data from RING_BUFFER_IO). Reading this register will clear it automatically.
Bit30	If the ring buffer bank state = 0, then bank A is writing, bank B is redable. If the ring buffer bank state = 1, then bank B is reading, bank A is readable.
Bit29～28	Ring buffer operation status

TRIG_IDLE	0x0	Stopped or waiting for start trigger.
TRIG_RUN	0x1	Collecting data.
TRIG_TURN	0x2	Wait for stop trigger.
TRIG_HIST	0x3	During dead time.

Bit27～16	Number of banks that collected data from the start of ring buffer operation to the present (1 bank = 1 ring buffer)
Bit15～11	always 0x0
Bit10～0	Address of ring buffer at stop (data after this is meaningless)

SCP1[RW] **Required**

Bit31～28	Signal conditioning settings for analog input channel 7. Set the following values according to the input type.
Bit28～24	Signal conditioning settings for analog input channel 6. Set the following values according to the input type.
Bit23～20	Signal conditioning settings for analog input channel 5. Set the following values according to the input type.
Bit19～16	Signal conditioning settings for analog input channel 4. Set the following values according to the input type.
Bit15～12	Signal conditioning settings for analog input channel 3. Set the following values according to the input type.
Bit11～8	Signal conditioning settings for analog input channel 2. Set the following values according to the input type.
Bit7～4	Signal conditioning settings for analog input channel 1. Set the following values according to the input type.
Bit3～0	Signal conditioning settings for analog input channel 0. Set the following values according to the input type.
	0x0 : Voltage ± 10 V 0x2 : Voltage ± 1 V, 4-20 mA (47 Ω) 0x4 : Voltage ± 100mV and thermocouple 0x6 : Voltage ± 10mV and thermocouple 0x3 : Platinum RTD 0x8 : 4096mV unipolar voltage *Acceleration XYZ (AI0-2), noise (AI3), barometric pressure (AI4), 1PPS (AI5) are also equivalent to 4096mV*
Default	0x0

SCP3[RW]

Bit0	Connect analog input to ground at 0, 1 for normal operation. If it is zero, the remaining analog input is an offset error, so by subtracting it, the zero error can be reduced.
Default	0x1

COUNTER[RW]

Bit31～29	Always 0
Bit28	Chattering cancellation setting (DI), value is valid at 1 and 0 is invalid.
Bit27～25	The operation mode of counter 3 is specified by the following 0 to 7. 0x0: 4x encoder counter, Z phase unused 0x1: 4x encoder counter, using Z phase 0x2: 2x encoder counter, Z phase unused 0x3: 2x encoder counter, using Z phase 0x4: 1x encoder counter, Z phase unused 0x5: 1x encoder counter, using Z phase 0x6: Up / down counter (pulse counter) Z phase unused 0x7: Up / down counter (pulse counter) Z phase used
Bit24～22	Specify the counter 2 operation mode. The setting contents are the same as the definition of Bit 27-25.
Bit21～19	Specify the counter 1 operation mode. The setting contents are the same as the definition of Bit 27-25.
Bit18～16	Specify the counter 0 operation mode. The setting contents are the same as the definition of Bit 27-25.
Bit15～14	The latch mode of the counter 3 is specified by the following 0 to 2. 0x0: Software latch 0x1: Latch when Z phase condition satisfied 0x2: Latch on Y phase rising edge
Bit13～12	Specifies the latch mode of counter 2. The setting contents are the same as the definition of Bit 15-14.
Bit11～10	Specifies the latch mode of counter 1. The setting contents are the same as the definition of Bit 15-14.
Bit9～8	Specifies the latch mode of counter 0. The setting contents are the same as the definition of Bit 15-14.
Bit7	Counter 3, Z phase condition satisfied mode (counter reset) is specified by the following 0 to 1. 0x1: Counter reset at rising of Z phase 1 + B phase 1 + A phase. 0x0: Counter reset at Z phase rising.

Bit6	Counter 2, Z phase condition satisfaction mode (counter reset) is specified. The setting contents are the same as the definition of Bit7.
Bit5	Counter 1, Z phase condition satisfaction mode (counter reset) is specified. The setting contents are the same as the definition of Bit7.
Bit4	Counter 0, Z phase condition satisfaction mode (counter reset) is specified. The setting contents are the same as the definition of Bit7.
Bit3	Used when software latch is specified in bits 15-14. 1 counter 3 reset, 0 non reset.
Bit2	Used when software latch is specified in bits 13-12. 1 counter 2 reset, 0 non reset.
Bit1	Used when software latch is specified in bits 11-10. 1 counter 1 reset, 0 non reset.
Bit0	Used when software latch is specified in bits 9-8. 1 counter 0 reset, 0 non reset.
Default	0x1000_0000 (only chattering canceler is on)

SETAO[RW]

Bit31～16	Analog output channel 1 (AO1) value.
Bit15～0	Analog output channel 1 (AO0) value.
Default	0x0

DO[RW]

Bit15～0	Set the digital output (DO) value.
Default	0x0

INFRS_PACK[RO] **Required(when not using RING_BUFFER_IO)**

Bit31～0 × 11	For the definition of 11 double word (44 bytes), refer to Page 4 read (block). Get 8ch analog input, 4ch counter / infrasound input, GPS, DI, temperature at a stretch.

RING_BUFFER_IO [RO] **Required (When not using INFRS_PACK)**

Bit31～0 × 1027	For the definition of 1027 double words (4108 bytes), refer to Page 4 reading (ring buffer). 8ch analog input x 128, 4ch counter / infrasound input x 128, GPS, DI, temperature can be acquired at at once.

LAST_BANK[RW]

Bit31～2	Always 0.
Bit1	Set to 1 to fix the readable ring buffer to bank B. Combined with Bit30 of BANK_CTC_ADDR, the final bank is acquired surely.
Bit0	When it is 1, the readable ring buffer is fixed to bank A. Combined with Bit30 of BANK_CTC_ADDR, the final bank is acquired surely.
Default	0x0